Course Type	Course Code	Name of Course	L	Т	P	Credit
DE	NECD532	Network On Chip	3	0	0	3

Course Objective

The objective of this course is to:

- Understand the concept of network on-chip
- Learn router architecture designs
- Study fault tolerance network on chip

Learning Outcomes

Upon successful completion of this course, the students will be able to:

- Compare different architecture design
- Discuss different routing algorithms
- Test and monitor the Fault Tolerance for Networks-on-Chip Infrastructures

Unit No.	Topics to be Covered	Lecture Hours	Learning Outcome
1	Introduction, OSI layer rules, Interconnection Networks, NetworkTopologies, Switching Techniques, Routing Strategies, Flow Control Protocol, Quality-of-ServiceSupport	07	The students will be introduced to the basic concepts of networks on chip.
2	Switching Techniques and Packet Format, Asynchronous FIFO Design, GALS Style of Communication	07	The students will learn different switching techniques.
3	Wormhole Router Architecture Design, VC Router Architecture Design, AdaptiveRouter Architecture Design.	07	The students will learn different switching techniques.
4	Packet routing, QoS, congestion control and flow control, router design, network link design, Efficient and Deadlock, Free Tree-Based Multicast Routing Methods	07	The students will learn the different routing algorithms on 1-D networks
5	Path-Based Multicast Routingfor 2D and 3D Mesh Networks, Fault-Tolerant Routing Algorithms, Reliable and Adaptive RoutingAlgorithms	07	The students will learn the routing algorithms on 2-D and 3-D networks
6	Design and Security in NOC, Formal Verification of Communications, Test and Fault tolerance, Monitoring Services for NOC.	07	The students will learn to Test and monitor the Fault Tolerance for Networks-on-Chip Infrastructures
	Total	42	

Text Books:

- 1. ChrysostomosNicopoulos, Vijaykrishnan Narayanan, Chita R.Das" Networks-on Chip "Architectures Holistic Design Exploration", Springer, 2010.
- 2. Fayezgebali, Haythamelmiligi, HqhahedWatheq E1-Kharashi "Networks-on-Chips theory and practice CRC press, 2009.

Reference Books:

- 1. Konstantinos Tatas and Kostas Siozios "Designing 2D and 3D Network-on-Chip Architectures" 2013
- 2. Palesi, Maurizio, Daneshtalab, Masoud "Routing Algorithms in Networks-on-Chip" 2014.
- 3. SantanuKundu, SantanuChattopadhyay "Network-on-Chip: The Next Generation of System on-Chip Integration",2014 CRC Press